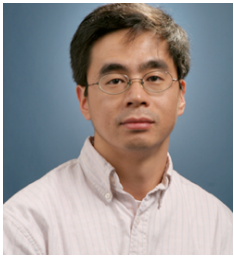


ARCHITECTURE LEVEL THERMAL MODELING, MANAGEMENT FOR MULTI-CORE AND 3D MICROPROCESSORS

ESRC SEMINAR

일시: 2013년 12월 10일(화) 오후 2:45 - 3:45

장소: 서울대학교 내 302동(제2공학관) 308호



Prof. Sheldon X.-D. Tan
(Univ. of California at Riverside)

Abstract

Temperature has become a major concern for high performance microprocessor and package design as more devices are integrated on a chip. This problem becomes more severe as the VLSI technology scales to the nanometer ranges. Excessively high on-chip temperature can cause many severe problems such as reduced reliability of chips and elevated cooling cost of the packaging. As a result, temperature modeling, analysis and runtime thermal management are critical to reduce hot spots, improve reliability for today's high performance multi-core microprocessors.

In this talk, I first review some recent research at MSLAB at UC Riverside for thermal analysis, modeling, and dynamic thermal management for multi-core and 3D microprocessors. Then I will present two recently proposed techniques. The first one is a new method for lateral resistance modeling of thorough silicon via (TSV) in 3D stacked ICs. We show that lateral thermal resistance is important for the overall thermal behavior of the 3D stacked ICs. I will present the lateral thermal resistance compact models will be presented and show that for TSV farm or TSV array, the thermal model are TSV-pitch dependent. In the second work, I will present a new dynamic thermal management scheme for reducing the temperature variations across the chip. Instead of intuitively assigning the heavy tasks to the low temperature cores to balance the thermal profile based on steady state thermal analysis, the new method applies moment matching based transient thermal analysis techniques for fast thermal estimation and prediction to guide the migration process. The resulting algorithm can lead to significant reduction of hot spots without full transient thermal simulation, which will benefit the system reliability. I will also show how this new transient thermal indicator can be computed in a distributed way for distributed thermal management.

Bio

Dr. Sheldon Tan received his B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China in 1992 and 1995, respectively and the Ph.D. degree in electrical and computer engineering from the University of Iowa, Iowa City, in 1999. He is a Professor in the Department of Electrical Engineering, University of California, Riverside, CA. He is the Associate Director of Compute Engineering Program (CEN) and cooperative faculty member in the Department of Computer Science and Engineering at UCR. Dr. Tan is also a Guest Professor of Shanghai Jiaotong University and the University of Electronic Science and Technology of China.

His research interests include statistical modeling, simulation and optimization of mixed-signal/RF/analog circuits, fast thermal analysis and modeling for microprocessors and platform systems, parallel circuit simulation techniques based on GPU and multicore systems, and embedded system designs based on FPGA platforms. Dr. Tan also co-authored three books: Symbolic Analysis and Reduction of VLSI Circuits published by Springer/Kluwer in 2005, Advanced Model Order Reduction Techniques for VLSI Designs by Cambridge University Press published in 2007 and Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Design by Springer Publishing in 2012. Dr. Tan served as an Associate Editor for three journals: ACM Transaction on Design Automation of Electronic Systems (TODAE), Integration, The VLSI Journal, and Journal of VLSI Design.

Dr. Tan received Outstanding Oversea Investigator Award from the National Natural Science Foundation of China (NSFC) in 2008. He received NSF CAREER Award in 2004. Dr. Tan received the Best Paper Award from 2007 IEEE International Conference on Computer Design (ICCD'07), the Best Paper Award from 1999 IEEE/ACM Design Automation Conference. He served as a technical program committee member for DAC, ICCAD, ASPDAC, ICCD, ISQED.

ESRC 센터장 장래혁 교수(1834), ESRC Administrator (1836)

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