A 5-day hands-on course:

Constructive Computer Architecture

(Website: http://cares.snu.ac.kr/bluespec2013)

Instructor: Professor Arvind (MIT)

Director of the Course: Prof. Jihong Kim (SNU)

Teaching Assistants: Sang-Woo Jun (MIT EECS Ph.D. Student),
Ming Liu (MIT EECS Ph.D. Student)

Place: Room 209, Building 302, Seoul National University

Date: 9:00am~5:00pm, July 8-12, 2013

후원: 서울대학교 차세대 임베디드 시스템을 위한 하드웨어/소프트웨어 통합 설계 환경 개발 사업단

Introduction:

Lectures and labs illustrate a constructive approach to computer architecture using a novel way of describing hardware. Introduction to Bluespec via combinational ALU and multi-cycle functional units. Bluespec concurrency model via in-order pipelined microarchitectures. Topics will include pipelines with multiple branch predictors; store buffers; blocking and non-blocking caches and superscalar architectures. Daily labs will provide students hands-on experience in designing various parts of the processor, which can be both simulated in software and synthesized to FPGAs and ASCIs. Time permitting, students will have a chance to run their own designs in FPGAs.

Instructor:

Arvind is the Johnson Professor of Computer Science and Engineering at the Massachusetts Institute of Technology (MIT) and a member of CSAIL (Computer Science and Artificial Intelligence Laboratory). From 1974 to 1978, prior to coming to MIT, he taught at the University of California, Irvine. Arvind received his M.S. and Ph.D. in Computer Science from the University of Minnesota in 1972 and 1973, respectively. He received his B. Tech. in Electrical Engineering from the Indian Institute of Technology, Kanpur, in 1969, and also taught there from 1977-78. Arvind has served on the editorial board of many journals including the Journal of Parallel and Distributed Computing, and the Journal of Functional Programming. He has chaired and served on the program committee of many meetings sponsored by ACM and IEEE. Arvind's current research interests are

synthesis and verification of large digital systems described using Guarded Atomic Actions; and Memory Models and Cache Coherence Protocols for parallel architectures and languages.

Prerequisites:

Introductory knowledge of Computer Architecture and Digital Design. Some familiarity with C++, Java or functional languages.

Daily Schedule:

	Contents Summary
Day 1 (July 8)	Lecture 1: Constructive Approach Lecture 2: Introduction to Bluespec via Combinational ALU Lecture 3: Multicycle Functional Units and Bluespec Modules
Day 2 (July 9)	Lecture 1: Pipelined Arithmetic Circuits Lecture 2: FIFOs and the Bluespec Concurrency Model Lecture 3: Concurrent Rule Scheduling
Day 3 (July 10)	Lecture 1: Non-Pipelined SMIPS Processor Lecture 2: Multicycle SMIPS Processor Lecture 3: Pipelining and Control Hazards
Day 4 (July 11)	Lecture 1: Data Hazards Lecture 2: Multistage Pipelines Lecture 3: Integrating Branch Predictors into the Pipeline
Day 5 (July 12)	Lecture 1: Caches Lecture 2: Superscalar Processors Lecture 3: Non-blocking Caches

Registration Information:

Please visit our course website: http://cares.snu.ac.kr/courses/bluespec2013/mainpage.htm

The registration deadline is **July 1, 2013**.

Note that the maximum number of attendees is limited to **20 people**.

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